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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/702,320	10/31/2000	Laurence R. Simar, Jr.	TI-30559	9784

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EXAMINER

HUISMAN, DAVID J

ART UNIT	PAPER NUMBER
2183	7

DATE MAILED: 09/09/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/702,320

Applicant(s)

SIMAR, JR. ET AL.
SL

Examiner

David J. Huisman

Art Unit

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*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --***Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 31 October 2000.

2a) This action is FINAL. 2b) This action is non-final.

3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-7 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) Claim(s) _____ is/are allowed.

6) Claim(s) 1-7 is/are rejected.

7) Claim(s) _____ is/are objected to.

8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.

10) The drawing(s) filed on 31 October 2000 is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) The proposed drawing correction filed on _____ is: a) approved b) disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.

12) The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.

14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) The translation of the foreign language provisional application has been received.

15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) Notice of References Cited (PTO-892)

2) Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) Information Disclosure Statement(s) (PTO-1449) Paper No(s) 5 and 6.

4) Interview Summary (PTO-413) Paper No(s). _____.
5) Notice of Informal Patent Application (PTO-152)
6) Other: _____

DETAILED ACTION

1. Claims 1-7 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: #3. Declaration as received on 2/5/2001, #4. Request to Correct Filing Receipts as received on 9, 4, 2001, #5. IDS as received on 9/4/2001, and #6. IDS as received on 4/11/2003.

Specification

3. The abstract of the disclosure is objected to because of the following minor informalities: Please remove reference labels 10, L1/2, S1/2, M1/2, D1/2, 700, 702, 704, and EP1...EP5. Also, "Figure 7B" should be removed from the end of the abstract. In line 5 (line 2 of the abstract), replace "includes" with either --including--, --that includes--, or --which includes--. Finally, it is requested that the abstract be modified to provide a little more detail (without exceeding 150 words) such that one would get a better idea of the content of the application by merely reading the abstract. Correction is required. See MPEP § 608.01(b).

4. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

5. The disclosure is objected to because of the following informalities: Please remove all attorney docket number references and provide application or patent numbers along with titles

when mentioning other related applications. Insert a comma after "computer" on page 3, line 12, after "systems" on page 4, line 10, and after ".D1" on page 12, line 20. On page 20, line 26, the examiner believes that the reference to "Figure 11" is incorrect (since Figure 11 deals with a cell phone and the specification is talking about phases of a pipeline). On page 11, line 5, and on page 23, the specification refers to figures that do not exist (Figure 2A, Figure 12, and Figure 13). On page 24, line 22, replace "611-613" with --610-613--. On page 25, line 23, replace "EP#(0)" with --EP3(0)--.

Appropriate correction is required.

Drawings

6. The drawings are objected to because of the following minor informalities: Two figures have been labeled "Figure 7A." The second should be relabeled as --Figure 7B--. Also, component 82 should be labeled in Fig.1. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

7. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: In Fig.1, labels 40b, 43, 82, 90, 100, and 102 have not been found by the examiner within the specification. In Fig.2, labels 40b, 12a,b, 14a,b, 16a,b, 18a,b, 210, 211, 212, 213, 214, 220, 221, 102, and 250 have not been found by the examiner within the specification. In Fig.8, label 822(0) has not been found by the examiner within the specification. In Fig.11, label 15 has not been found by the examiner within the specification. Also within Fig.11, "10/40" can be replaced with --40--. A proposed

drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

8. Claims 4-6 are objected to because of the following informalities: It is recommended that applicant replace "The digital system" with --The digital processing system-- in each of the claims 4-6 for consistency with claims 1-3. Appropriate correction is required.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

10. Claims 1-5 and 7 are rejected under 35 U.S.C. 102(e) as being anticipated by

Sharangpani et al., U.S. Patent No. 6,237,077 (herein referred to as Sharangpani).

11. Referring to claim 1, Sharangpani has taught a digital processing system having a microprocessor, wherein the microprocessor comprises:

a) fetch circuitry for fetching instruction fetch packets, wherein each fetch packet contains a first plurality of instructions. See Fig. 3 and note that instruction buffer 320 holds fetch packets

(which are fetched by fetch circuitry). These fetch packets contain a first plurality of instructions. See Fig.2.

b) a second plurality of functional units, the plurality of functional units operable to execute a second plurality of instructions in parallel. See Fig.3 and note the plurality of functional units (M0, M1, I0, I1, F0, F1, and BR0-BR2). These units receive a second plurality of instructions that have been fetched in order to execute them in parallel. See column 3, lines 64-66 (note that an instruction group refers to instructions that can be executed in parallel).

c) dispatch circuitry operable to select an execution packet from one or more fetch packets, wherein an execute packet varies in size and contains only a set of instructions that can be executed in parallel on the plurality of functional units, whereby a first execute packet contains a different number of instructions than a second execute packet due to resource constraints. It should be realized from Fig.2 that each fetch packet includes a stop field and a template field. The stop field of a first packet indicates whether or not inter-group dependencies exist between the first packet and the next packet. See column 4, lines 4-5. More specifically, if the stop field indicates that no group boundary exists between fetch packets, then instructions from multiple fetch packets are considered to be in the same group (thereby creating a larger execution packet), and instructions in the same group are executed in parallel. On the other hand, looking at column 5, lines 44-45, and Table 2 in column 6, it can be seen that the template field indicates that some fetch packets include intra-packet boundaries (denoted by the vertical parallel lines). When this occurs, instructions in the same fetch packet are divided into multiple execution packets (limiting the size of an execution packet). With this in mind, it can be seen that the size of an execution packet can vary (it can grow if multiple fetch packets are in the same group).

(denoted by the stop bit) or it can be smaller than the size of a fetch packet if intra-packet boundaries exist (denoted by the template field)). Dispatch circuitry (Fig.3, components 330 and 340) will check the stop field and template field for each fetch packet, for instance, and route the instructions appropriately. See column 7, lines 59-62.

12. Referring to claim 2, Sharangpani has taught a digital processing system as described in claim 1. Sharangpani has further taught that the first plurality is equal in number to the second plurality. For instance, see Fig.3 and column 7, lines 25-32, and note that there are three branch execution units (BR0-BR2). By providing three branch execution units, up to three branch instructions will be executed in parallel. It should be further noted from Table 2 in column 6 that three branch instructions will be provided to all three branch execution units in the case of instruction template B, where three branch instructions exist within one fetch packet (and execution packet).

13. Referring to claim 3, Sharangpani has taught a digital processing system as described in claim 1. Sharangpani has further taught that a first execute packet spans a first fetch packet and a second fetch packet. As described in the rejection of claim 1, each fetch packet includes a stop field. The stop field of a first packet indicates whether or not inter-group dependencies exist between the first packet and the next packet (second packet). See column 4, lines 4-5. More specifically, if the stop field indicates that no group boundary exists between fetch packets, then instructions from multiple fetch packets are considered to be in the same group (thereby creating a larger execution packet), and instructions in the same group are executed in parallel. For instance, from Table 2 in column 6, assume that a first fetch packet corresponds to template 6 and a second fetch packet corresponds to template B. If there are no dependencies (no boundary)

between the two packets (denoted by the stop field), then those two packets will be combined into a single instruction group. All of the instructions from those two fetch packets would make up a single execution packet, where each of the instructions in the execution packet will be executed in parallel. This is an example of how an execute packet spans multiple fetch packets.

14. Referring to claim 4, Sharangpani has taught a digital processing system as described in claim 3. Sharangpani has further taught that the dispatch circuitry comprises:

- a) a first latch to hold the first fetch packet. See Fig.3, components 312(0)-312(2).
- b) a second latch to hold the second fetch packet. See Fig.3, components 312(3)-312(5).
- c) selection circuitry to select a first portion of the first execute packet from the first latch and a second portion of the first execute packet from the second latch. It should be noted that if a first fetch packet's stop field indicates that there are no inter-group dependencies with a second fetch packet, then instructions from both fetch packets will be selected by the selection circuitry (Fig.3, component 340) from their latches for execution. See column 7, lines 59-62.

15. Referring to claim 5, Sharangpani has taught a digital system as described in claim 4. Sharangpani has further taught that the dispatch circuitry further comprises control circuitry connected to a plurality of instruction positions corresponding to the plurality of instructions of a fetch packet in the first latch and in the second latch to determine a boundary of each execute packet, the control circuitry operable to control the selection circuitry in response to an execute packet boundary. See Fig.3, and column 7, lines 59-62. Note that the control circuitry 330 reads the template (and by doing so, determines the group boundary) and indicates to the selection circuitry to select the appropriate instructions and route them to the execution units for parallel execution.

16. Referring to claim 7, Sharangpani has taught a method of operating a digital system having a microprocessor, wherein the microprocessor has a plurality of functional units for executing instructions in parallel, comprising the steps of:

- a) fetching a sequence of instruction fetch packets, wherein each fetch packet contains a first plurality of instructions. See Fig.3 and note that instruction buffer 320 holds fetch packets (which are fetched by fetch circuitry). These fetch packets contain a first plurality of instructions. See Fig.2.
- b) examining each fetch packet to determine an execution packet boundary. It should be realized from Fig.2 that each fetch packet includes a stop field and a template field. The stop field of a first packet indicates whether or not inter-group dependencies exist between the first packet and the next packet. See column 4, lines 4-5. More specifically, if the stop field indicates that no group boundary exists between fetch packets, then instructions from multiple fetch packets are considered to be in the same group (thereby creating a larger execution packet), and instructions in the same group are executed in parallel. On the other hand, looking at column 5, lines 44-45, and Table 2 in column 6, it can be seen that the template field will indicate that a given fetch packet include intra-packet boundaries (denoted by the vertical parallel lines). When this occurs, instructions in the same fetch packet are divided into multiple execution packets (limiting the size of an execution packet). With this in mind, it can be seen that the size of an execution packet can vary (it can grow if multiple fetch packets are in the same group (denoted by the stop bit) or it can be smaller than the size of a fetch packet if intra-packet boundaries exist (denoted by the template field)). Dispatch circuitry (Fig.3, components 330 and 340) will examine the

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stop field and template field of each fetch packet, for instance, in order to determine where and when to route instructions. See column 7, lines 59-62.

c) selecting a first portion of an execute packet from a first fetch packet and a second portion of a first execute packet from a second fetch packet if the first execute packet boundaries span the first fetch packet and the second fetch packet. As described in the rejection of claim 1, each fetch packet includes a stop field. The stop field of a first packet indicates whether or not inter-group dependencies exist between the first packet and the next packet (second packet). See column 4, lines 4-5. More specifically, if the stop field indicates that no boundary exists between fetch packets, then instructions from multiple fetch packets are considered to be in the same group (creating a larger execution packet), and instructions in the same group are executed in parallel. For instance, from Table 2 in column 6, assume that a first fetch packet corresponds to template 6 and a second fetch packet corresponds to template B. If there are no dependencies between the two packets (denoted by the stop field), then those two packets will be combined into a single instruction group. All of the instructions from those two fetch packets would make up a single execution packet, where each of the instructions in the execution packet will be executed in parallel. This is an example of how an execute packet spans multiple fetch packets.

Claim Rejections - 35 USC § 103

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

18. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sharangpani, as applied above, in view of Haataja, U.S. Patent No. 6,137,836.

19. Referring to claim 6, Sharangpani has taught a digital system as described in claim 5. Sharangpani has not taught that the digital system is a cellular telephone comprising the components set forth in claim 6. However, Haataja has taught a cellular telephone comprising:

- a) an integrated keyboard connected to the processor via a keyboard adapter. See Fig.8, component 72.

- b) a display, connected to, the processor via a display adapter. See Fig.8, component 36.

- c) radio frequency (RF) circuitry connected to the processor. See Fig.8, component 56, and column 7, lines 6-11.

- d) an aerial connected to the RF circuitry. See Fig.8, component 54.

It should be realized that Sharangpani has taught a processor which processes branch instructions more efficiently, thereby improving the performance of the processor. See column 1, lines 66-

67. A person of ordinary skill in the art would have recognized that an improved processor would lead to the overall improvement of the device in which it is embedded. As shown in Fig.8 of Haataja, and, as is well known in the art, cellular telephones are controlled by some sort of processor. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have the incorporate the digital system of Sharangpani into a cell phone, as taught by Haataja, in order to improve the overall performance of the cell phone.

Conclusion

20. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

Hull et al., U.S. Patent No. 5,922,065, has taught a processor utilizing a template field for encoding instruction sequences in a wide-word format. This reference is similar to Sharangpani but includes more information on the boundaries and the stop and template fields while providing less information on how these instructions are dispersed and executed.

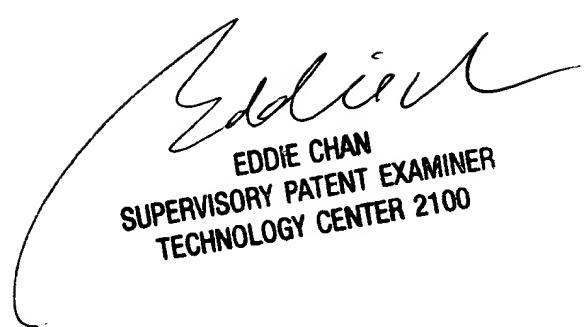
Arnold et al., U.S. Patent No. 6,470,445, has taught preventing write-after-write data hazards by canceling earlier write when no intervening instruction uses value to be written by the earlier write. In addition, Arnold has taught instruction bundles which include stop bits for grouping purposes.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David J. Huisman whose telephone number is (703) 305-7811. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

DJH
David J. Huisman
September 3, 2003



Eddie Chan
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100